Are You a Junior Verification Engineer?

SyoSil is a leading consulting company holding broad expertise within the field of System-on-Chip and ASIC/FPGA solutions, collaborating with clients being the top European and U.S. semiconductor companies.

What do we offer?
We are looking for several recently graduated/junior engineers within the field of digital electronics and computer science to strengthen our teams.
At SyoSil we have a proven successful record of hiring and training young talents and shape them into self-managed, high-performing and experienced Digital Design and Verification engineers.
We will educate you – based on your current knowledge – in the most recent and exciting fields of the industrial IC flow, with focus on functional verification using languages and methodologies such as SystemVerilog/UVM, Coverage Driven & Constrained Random Verification, Assertions and Formal Property Checking.

And now, we are hiring. Are you joining us?

At SyoSil, you will

- Start learning on internal projects, accompanied by an experienced tutor that will guide you through the learning processenv cfg obj
- Grow into a confident verification engineer capable of analyzing, architecting, and implementing verification environments to thoroughly test complex IPs using industry standards as SystemVerilog/UVM
- Join one of our teams working on exciting projects using bleeding-edge technologies with one of our high-profile clients

To fit the role, we expect you to have

- Knowledge of the basic ASIC/FPGA development flow
- Knowledge of Linux environments
- Good English communication skills, both written and verbal
- Degree in Electronics, Telecommunications, Computer Science or Mathematics
- Experience with any of below is a plus:

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- Hardware description languages: VHDL, Verilog or SystemVerilog
- Object-oriented programming
- Scripting: Shell, Python.
- Familiarity with revision control tools (e.g. GIT)

Why should you apply?
At SyoSil we offer a competitive salary and a flexible working environment meeting your personal work-life balance expectations. We invest significantly in the knowledge and expertise of the SyoSil team, making it possible for you to develop and maintain first class professional skills. We encourage personal development and we are eager for you to propose your ideas and carry on with any personal interest and project you might have.

We are a young and dynamic team of 30+ full time engineers working in an international environment, with very skilled and open-minded colleagues. Our headquarters are located less than 15 minutes by train from downtown Copenhagen. We will support you in the relocating process if you are traveling from abroad.

Are you interested?

Send us your application, CV and your university transcript.

We can't wait to welcome you at SyoSil and do great things together.

For any additional information, do not hesitate to contact us:
Jacob Sander Andersen (CTO), Email: jacob@syosil.com

SyoSil is a leader in FPGA/ASIC design and verification solutions, including device firmware and tool development. We advice our clients on how to improve their design and verification methodologies and deliver turn-key verification flows and Verification IP, based on industry standards such as SystemVerilog/UVM. Our clients include top European and U.S. semiconductor companies, all being respective leaders in their respective product segments (consumer, communication, automotive and surveillance).

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